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REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed September 25, 2003. Claims 70-81, 94-95 and 101-122 were pending in the application. Applicants have cancelled claims 94-95. Applicants assert that claims 70-81 and 101-122 are in condition for allowance and respectfully request entry of the present Response C and consideration of these claims.

I. Rejection of Claims 70-81, 94-95, and 101-122 under 35 U.S.C. § 102(e)

The Examiner rejected claims 70-81, 94-95, and 101-122 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,557,145 ("*Boyle*"). Applicants have cancelled claims 94-95. Because *Boyle* does not disclose each of the limitations of claims 70-81 and 101-122, Applicants respectfully submit that these claims are in condition for allowance.

A. Claims 101-107

Applicants assert that *Boyle* does not disclose each of the limitations of claim 101, and thus, does not anticipate claim 101. Claim 101 includes, among other limitations, "creating a physical prototype ... creating a physical design ... said creating of a physical prototype is performed prior to said creating of said physical design." Because *Boyle* does not disclose creating a physical prototype prior to creating the physical design, as recited in above in claim 101, Applicants submit that claim 101 is patentable over the cited art.

Boyle provides "a method for optimizing a layout design, which minimizes the optimization cycle by incorporating interconnect wiring delays and performing logic optimization in the placement and routing operations." *Boyle*, col. 3, ll. 23-26. As illustrated by Figures 1-3 and the accompanying description, *Boyle* is concerned with placement and routing operations and incorporating logic optimization into these operations. Placement and routing, as taught by *Boyle*, is similar to the placement and routing performed by the physical design tool described in Applicants' specification. *See, e.g.*, *Specification*, pg. 1, ll. 8-26, Figure 1. Thus, *Boyle* discloses creating a physical design. *Boyle*, however, does not disclose "creating of a physical prototype ... prior to creating of said physical design," as recited in claim 101.

As cited by the Examiner, *Boyle* teaches, "[t]his optimization cycle is repeated until all timing problems are resolved, represented by the post-layout sign-off step 114. Test patterns can then be generated in an automatic test pattern generation (ATPG) step 116, and the final layout can then be manufactured." *Boyle*, col. 2, ll. 45-50. Applicants respectfully submit that this language does not disclose "creating post-layout or 'physical prototype' in terms of Application, and final layout or 'physical design'" or "[p]ost-layout/'physical prototype' is created prior final layout/'physical design,'" as asserted by the Examiner. *Office Action*, p. 10, ¶ 6.

Applicants respectfully submit that the Examiner is mis-interpreting the cited language of *Boyle* and that this language does not disclose a physical prototype that is created prior to "creating of said physical design," as recited in claim 101. The "post-layout," as cited by the Examiner, is not a layout or design at all, but rather a step in the method described by *Boyle*. *Boyle* clearly recites that the optimization cycle is repeated until all timing problems are resolved, "represented by the post-layout sign-off step 114." *Boyle*, col. 2, l. 45 (*emphasis added*). *Boyle* is merely describing that once a designer is satisfied with a layout design generated through the iterative method, and all timing problems are resolved, a sign-off step is performed that is post-layout (i.e., after layout step 112). *Boyle* is not describing a post-layout and a final layout, but merely the manufacture of a final layout after performance of a sign-off step that is "post-layout," or after layout is performed (step 112).

The Examiner additionally cites the description of method 200 in *Boyle* for the disclosure of "creating of a physical prototype ... prior to creating of said physical design," as recited in claim 101. As with the section discussed above, however, *Boyle* describes a "post-layout sign-off step 114," not a "post layout" that is created prior to a "final layout," as asserted by the Examiner. *Boyle*, col. 5, ll. 28-31. *Boyle* is directed to and describes the creation of a physical design through an iterative method. *Boyle*, however, does not disclose "creating of a physical prototype ... prior to creating of said physical design," as recited in claim 101.

Claim 101 further recites that "creating of a physical prototype includes ... tracking an error in said predicting of timing." Applicants assert that *Boyle* does not disclose "tracking an error in said predicting of timing."

Boyle describes the extraction of "estimates of timing parameters." *Boyle*, col. 2, ll. 3-4. After placing and routing cells, a timing analysis step is performed on the routed layout design to

determine if there are any "timing problems in some signal paths." *Id.* at ll. 35-40. This portion of *Boyle* simply discloses a timing estimate and a timing analysis to uncover timing problems. *Boyle* does not disclose tracking an error in a prediction or estimate itself. *Boyle* also discloses that "[b]uffer insertion based on these criteria can be performed while delay or slack graphs are calculated" and "a statistical estimate of delay is provided for each net within a quanto-cluster." *Boyle*, col. 9, ll. 65-67; col. 11, ll. 10-13. These portions of *Boyle* merely describe a statistical estimate of delay, not tracking an error in the estimate.

As described in Applicants' specification with respect to one embodiment, a "histogram that plots the length of wires versus instances of net for the bin" is created. *Specification*, p. 8, l. 31 – p. 9, l. 1. An "error calculation tool 56 calculates the errors in the prediction of the timing value (the "error prediction") in the bin from the mean and standard deviation of the wire lengths." *Id.* at p. 9, ll. 2-5. The error is the error in the prediction itself caused by the possible distribution of wire lengths. This is not an error determined by comparing a prediction with an actual end result. Accordingly, as recited in claim 101, "an error in said predicting of timing" is tracked. (*Emphasis added*). *Boyle* does not disclose tracking or determining an error in predicting. *Boyle* merely describes estimates of timing parameters, the determination of timing problems from a timing analysis, and a statistical estimate of delay. Such a description does not disclose "tracking an error in said predicting," as recited in claim 101.

Applicants further assert that the other portions of *Boyle* cited against the limitation including "tracking an error in said predicting of timing" do not disclose this limitation as discussed below.

i. col. 1, ll. 24-27

This is the field of the invention. There is no mention of tracking an error in a prediction of timing.

ii. col. 2, ll. 13-20

This section describes a front-end processing step, a pre-layout signoff step, and a layout step. There is no mention of tracking an error in a prediction of timing.

iii. col. 3, ll. 51-67; col. 4, ll. 1-4

This section describes a parallel processing design automation system implementation of the method of *Boyle's* invention. Timing analysis is mentioned. There is no mention, however, of tracking an error in a prediction of timing.

iv. col. 4, ll. 54-58

This section describes interconnect congestion and a cost function that is a combination of timing and physical design area. There is no mention of tracking an error in a prediction of timing.

v. col. 5, ll. 7-17

This section describes a design method including a timing analysis step. There is no mention of tracking an error in a prediction of timing.

vi. col. 20. ll. 62-67; col. 21, ll. 1-16

This section covers two claims reciting a storage device including code for performing a method. One step of the method includes performing a timing analysis. There is no mention of tracking an error in a prediction of timing.

Because *Boyle* does not disclose each of the limitations of claim 101, Applicants assert that claim 101 is patentable over the cited art. Claims 102-107 each ultimately depend from claim 101, and should be patentable over the cited art for at least the reasons set forth above with respect to claim 101. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 101-107 under 35 U.S.C. § 102(e).

B. Claims 108-112

Claim 108 recites, "creating of a physical prototype is performed prior to said step of providing [said physical prototype for a physical design process so that a physical design can be created]." As set forth above with respect to claim 101, *Boyle* does not disclose "creating a physical prototype ... creating a physical design ... said creating of a physical prototype is

performed prior to said creating of said physical design." Thus, for the same reasons as set forth with respect to these limitations of claim 101, Applicants assert that *Boyle* does not disclose each of the limitations of claim 108. Claims 109-112 each ultimately depend from claim 108 and should be patentable for at least the same reasons set forth with respect to claim 108. Accordingly, Applicants assert that claims 108-112 are patentable over the cited art and request withdrawal of the rejection under 35 U.S.C. § 102(e).

C. Claims 113-117

Claim 113 recites a computer-readable medium including computer code configured to perform the design of an integrated circuit, wherein "creating of a physical prototype is performed prior to said step of providing [said physical prototype for a physical design process so that a physical design can be created]." As set forth above with respect to claim 101, *Boyle* does not disclose "creating a physical prototype ... creating a physical design ... said creating of a physical prototype is performed prior to said creating of said physical design." Thus, for the same reasons as set forth with respect to these claim limitations of claim 101, Applicants assert that *Boyle* does not disclose each of the limitations of claim 113. Claims 114-117 each ultimately depend from claim 113 and should be patentable for at least the same reasons set forth with respect to claim 113. Accordingly, Applicants assert that claims 113-117 are patentable over the cited art and request withdrawal of the rejection under 35 U.S.C. § 102(e).

D. Claims 118-122

Claim 118 recites "creating of a physical prototype is performed prior to said step of providing [said physical prototype for a physical design process so that a physical design can be created]." As set forth above with respect to claim 101, *Boyle* does not disclose "creating a physical prototype ... creating a physical design ... said creating of a physical prototype is performed prior to said creating of said physical design." Thus, for the same reasons as set forth with respect to these claim limitations of claim 101, Applicants assert that *Boyle* does not disclose each of the limitations of claim 118. Claims 119-122 each ultimately depend from claim 118 and should be patentable for at least the same reasons set forth with respect to claim

118. Accordingly, Applicants assert that claims 118-122 are patentable over the cited art and request withdrawal of the rejection under 35 U.S.C. § 102(e).

E. Claims 70-75

Claim 70 recites "receiving a sign-off prototype," and "after receiving the sign-off prototype ... generating a second physical design of the circuit from the sign-off prototype." Claim 70 further recites, "tracking an error in prediction of a timing value." Thus, for the same reasons as set forth above with respect to claim 101, Applicants assert that *Boyle* does not disclose each of the limitations of claim 70. Claims 71-75 each ultimately depend from claim 70 and should be patentable for at least the same reasons set forth with respect to claim 70. Accordingly, Applicants assert that claims 70-75 are patentable over the cited art and request withdrawal of the rejection under 35 U.S.C. § 102(e).

F. Claims 76-81

Claim 76 recites a semiconductor device manufactured by "receiving a sign-off prototype" and "after receiving the sign-off prototype ... generating a second physical design of the circuit from the sign-off prototype." Claim 76 further recites, "tracking an error in prediction of a timing value." Thus, for the same reasons as set forth above with respect to claim 101, Applicants assert that claim 76 is patentable over the cited art. Claims 77-81 each ultimately depend from claim 76 and should be patentable for at least the same reasons set forth with respect to claim 76. Accordingly, Applicants assert that claims 76-81 are patentable over the cited art and request withdrawal of the rejection under 35 U.S.C. § 102(e).

II. Conclusion

In view of the above Remarks, reconsideration of claims 70-81 and 101-122 is respectfully requested.

The undersigned respectfully requests an interview with the Examiner to discuss the claims prior to the issuance of any action in reply to the present Response C. Accordingly, an interview request form is submitted herewith. The Examiner is invited to call the undersigned at anytime to conduct or schedule the interview.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this document, including any fee for extension of time, which may be requested.

Respectfully submitted,

Date: 11/21/03 By: _____

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